

AMENDMENT TO THE CLAIMS:

This listing of claims will replace all prior listings of claims in the application:

LISTING OF CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) An isolation trench in a substrate material for electrically insulating high voltage power elements ~~(7)~~ integrated in combination with low voltage logic elements ~~(6)~~ into the same silicon circuit in a substrate wafer (trench isolation), said trench being partially filled with electrically insulating material and partially with a fill material, said trench extending to an electrically insulating layer ~~(2)~~ located at least at the bottom of said trench, wherein
 - (i) within said trench ~~(1)~~ an alternating sequence or alternatingly electrically insulating layers (insulation layers) and fill layers ~~(4a, 5a, 9a, 10, 4b, 5b, 9b)~~ are provided with a parallel orientation with respect to trench walls;
 - (ii) the plurality of insulating layers and fill layers ~~(4a, 4b, 5a, 5b, 9a, 9b, 10)~~ are composed such that with respect to a sum over all parallel layers within said trench ~~(1)~~ a coefficient of thermal expansion of the sum of layers is adjusted so as to be at least close to a coefficient of expansion of the substrate materials ~~(1, 3)~~, thereby avoiding a bending of the substrate wafer.
2. (Currently Amended) An isolation trench according to claim 1, wherein the insulating layers ~~(4a, 4b)~~ are comprised of silicon dioxide.

3. (Currently Amended) An isolation trench according to claims 1 or 2, wherein the plurality of fill layers ~~(5a, 5b, 10)~~ comprise polysilicon within their base material.
4. (Currently Amended) An isolation trench according to claim 1, wherein the entire trench ~~(T)~~ in said substrate material is filled with said insulating layers and fill layers.
5. (Original) An isolation trench according to claim 1, wherein said coefficients of thermal expansion are adapted to each other in such a way that an inadvertent bending of the substrate wafer (upon thermal stress) is avoided.
6. (Currently Amended) An isolation trench according to claim 1, wherein at least seven parallel layers are provided within said trench-~~(T)~~.
7. (Currently Amended) An isolation trench according to claim 1, wherein the inner most layer ~~(10)~~ of the filled trench is a fill layer.
8. (Currently Amended) An isolation trench according to claim 1, wherein all of the layers within said trench ~~(T)~~ are exposed at the trench top surface and are particularly planarized or smoothed.
9. (Currently Amended) An isolation trench within a substrate material ~~(1, 3)~~ of a substrate wafer for laterally electrically insulating (trench isolation) a first active semiconductor area-~~(7)~~ provided for the formation of a high voltage power element, with respect to a second active semiconductor area-~~(6)~~, provided for the formation of at least one low voltage logic element, both elements being commonly integrated into the same silicon circuit, said trench-~~(T)~~ extending down to an electrically insulating layer ~~(2)~~ that is at least located at a bottom of

said trench-(T), said electrically insulating layer (2) preferably being provided below said active areas (6, 7) for a vertical electrical insulation, wherein

- (a) within said trench-(T) an alternating sequence of or alternately electrically insulating layers (insulation layers) and fill layers (4a, 5a, 9a, 10, 4b, 5b, 9b) are provided in a substantially parallel orientation with respect to trench walls;
 - (b) the plurality of insulating layers and fill layers (4a, 4b, 5a, 5b, 9a, 9b, 10) are composed and configured such that in a sum over all parallel layers provided within said trench-(T), a first coefficient of thermal expansion of the layer stack is adjusted so as to be at least close to a second coefficient of expansion of the substrate materials (1, 3) so as to at least reduce and preferably substantially completely avoid bending of the substrate wafer upon thermal stress.
10. (Currently Amended) A method of manufacturing at least one isolation trench (T)-for electrically insulating high voltage power elements-(7), which are integrated into the same silicon circuit along with low voltage logic elements-(6), said trench (T)-being filled to a first part with electrically insulating material and to a second part with a fill material in the form of layers, said trench extending to or into an electrically insulating layer-(2), wherein
 - (i) after depositing a first insulating layer (4a, 4b)-covering trench walls, a first fill layer (5)-is incorporated and restricted (5a, 5b)-such that the fill layer (5)-is not present on a trench bottom-(B1);
 - (ii) thereafter a second insulating layer (9a, 9b)-and following this layer a second fill layer (10)-is incorporated into said trench-(T);

- (iii) a planarization and smoothing (planarizing) of at least a trench surface (12) is performed.
11. (Currently Amended) A method according to claim 10, wherein silicon dioxide layers (4a, 4b, 9a, 9b) are incorporated into said trench (T) as insulating layers.
12. (Currently Amended) A method according to claim 10, wherein such layers are incorporated into said trench (T) as fill layers (5a, 5b, 10), which comprise polysilicon in their base material.
13. (Currently Amended) A method according to claim 10, wherein at least one of the insulating layers (9a, 9b) is formed by oxidizing the fill layers (5a, 5b) comprising polysilicon within their base material.
14. (Currently Amended) A method according to claim 10, wherein a finally formed insulating layer is used as a stop layer for removal of an overlying layer at a lateral portion (4c, 9a', 9b') outside of said trench.
15. (Currently Amended) A method according to claim 14, wherein said stop layer (4c, 9a', 9b') reduces an etch rate after an etch removal of an overlying lateral portion (10a, 10b) of the last fill layer.
16. (Currently Amended) A method according to claim 10, wherein the exposed trench bottom (B1), after restricting the first fill layer (5) into two lateral layer portions (5a, 5b) extending substantially parallel to the trench walls, has less a width compared to a width of a trench bottom (B0) prior to the fill step or a width of an initial trench bottom (B).

17. (Currently Amended) A method according to claim 10, wherein, depending on a magnitude of the voltage to be blocked, a sequence is continued until said trench ~~(T)~~ is completely filled by alternatingly incorporating insulating layers and fill layers.
18. (Currently Amended) A method according to claims 17 and 10, wherein at least two further insulating layers ~~(9a, 9b)~~ and at least one further fill layer ~~(10)~~ are incorporated by restricting the previously incorporated fill layer ~~(5)~~.
19. (Currently Amended) A method according to claim 18, wherein the step of restriction is accomplished by opening the fill layer ~~(5)~~ down to the bottom ~~(2, B4)~~ of the trench, for forming new vertical trench walls.
20. (Original) A method according to claim 19, wherein the new trench walls are more closely spaced to each other and more closely disposed at the center of the trench compared to previously existing trench walls which are covered with the previously incorporated insulated layers.
21. (Currently Amended) An isolation trench according to claims 1 or 9, wherein the insulating layers ~~(4a, 4b; 9a, 9b)~~ within said trench ~~(T)~~ are formed of different materials or at least some of the layers are formed of different materials.